Sea of Polymer Pillars: Compliant Wafer-Level Electrical–Optical Chip I/O Interconnections

Muhannad S. Bakir, Thomas K. Gaylord, Kevin P. Martin, and James D. Meindl

***Abstract*—An electrical–optical chip input–output (I/O) interconnection technology called sea of polymer pillars (SoPP) is presented. SoPP provides highly process-integrated and mechanically flexible (compliant) electrical–optical die-to-board interconnections that mitigate thermo-mechanical expansion mismatches. The I/O density of SoPP exceeds $10^5/\mathrm{cm}^2$. The compliance of the polymer pillars is shown to be 3–5 μm/mN. Approximately 50% input optical coupling efficiency into a volume grating coupler through a set of polymer pillars is demonstrated.**

***Index Terms*—Interconnections, optical polymers, optical waveguides, packaging, waveguide discontinuities.**

I. Introduction

A WELL-KNOWN side effect of Moore's law is the interconnect problem, which asserts that the performance limitations of a microsystem will not be imposed by the transistors performing computational functions but rather by the interconnection networks performing communication functions [1]. Moore's law has fueled the need for enormous communication bandwidth; the projected chip-to-board [input–output (I/O)] communication frequency at the 22-nm technology node (year 2016) is 28.751 GHz [2]. Microphotonic devices and interconnects can potentially greatly enhance the performance of a microsystem by leveraging high-bandwidth, low-latency, crosstalk-resilient, and low-power communication networks [1], [3]–[5]. However, these optical interconnects must be integrated with electrical interconnects needed for at least the chip's current supply. The focus of this letter is to introduce an I/O interconnection technology that provides the ability to simultaneously deliver electrons and photons between the die and the board.

Sea of polymer pillars (SoPP) is a highly process integrated I/O interconnection system. SoPP enables wafer-level batch fabrication of electrical, optical, and dual-mode electrical–optical I/O interconnections [6]. SoPP is the second generation of sea of leads I/O interconnection technology [7], a first approach to an integrated electrical–optical I/O interconnection system. SoPP provides high tolerance to offsets that are caused by coefficient of thermal expansion (CTE) mismatches between the die and the board through mechanically flexible (compliant) I/O interconnections.

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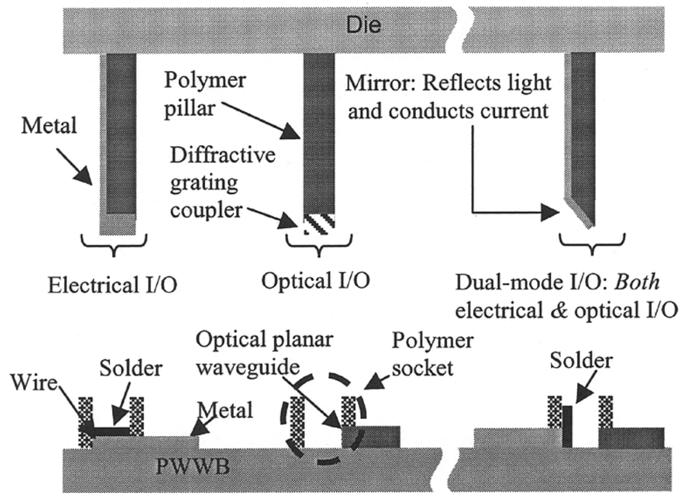

Fig. 1. Electrical, optical, and dual-mode I/O interconnections through SoPP. Dual-mode polymer pillar I/Os provide simultaneous electrical and optical interconnections. Optically compatible adhesives are used to make the mechanical interconnections needed for the optical I/Os.

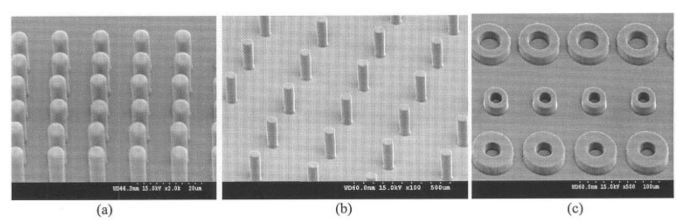

Fig. 2. SEM micrographs of polymer pillars, with a wide range of dimensions and polymer sockets. (a) The pillars are 13 μm tall, 5 μm wide, and on a 12-μm area-array pitch. (b) The pillars are 170 μm tall, 55 μm wide, and on a 325-μm area-array pitch. (c) The sockets are 13 μm tall.

II. SoPP Electrical–Optical I/O Interconnect Configurations and Fabrication

SoPP provides matching mechanical connections between the die and the board, as schematically illustrated in Fig. 1. On the die side, surface-normal optical waveguides, or polymer pillars, are batch fabricated above optical devices–elements (detectors, sources, mirrors, gratings, etc.), while on the printed wiring–waveguide board (PWWB), polymer sockets are batch fabricated to hold and align the pillars to the board. Scanning electron microscope (SEM) micrographs of a set of polymer pillars and polymer sockets are shown in Fig. 2. Each polymer pillar (or polymer pin) acts as the waveguide core with the air surrounding it acting as the waveguide cladding. This results in a high index of refraction difference (Δn) between the core and the cladding. In order to facilitate surface-normal optical coupling between the polymer pillars and the board-level

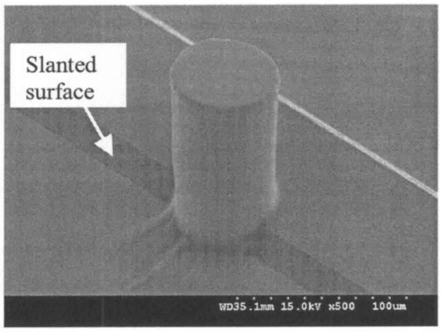

Fig. 3. SEM micrograph of a 100-μm-tall and 55-μm-wide polymer pillar fabricated on a slanted surface to ultimately facilitate optical surface-normal coupling between a planar waveguide and a polymer pillar. Planar waveguide is not shown.

optical planar waveguides, mirrors and diffractive grating couplers are fabricated either on the tips of the polymer pillars (Fig. 1) or on the board-level waveguides. Fig. 3 is an SEM micrograph of a polymer pillar fabricated on a slanted surface (mirror) to ultimately facilitate surface-normal optical coupling between a planar waveguide and the polymer pillar waveguide. It is possible to create dual-mode, or heterogeneous, I/O interconnections where each polymer pillar provides simultaneous electrical and optical interconnection. One example of such a dual-mode polymer pillar is shown in the schematic of Fig. 1. The metallized surface of the polymer pillar's slanted tip is a mirror that reflects an optical signal from the PWWB level waveguide into the polymer pillar while the metal film on the pillar's sidewall provides electrical interconnection. Thus, this I/O structure represents the highest level of electrical and optical interconnect process integration. The thickness of the metal deposited on the polymer pillars is selected such that it provides low-parasitic electrical interconnections and does not disturb the highly compliant nature of the polymer pillars. In addition, the metal film partially covering the dual-mode polymer pillars has to be highly reflective at the wavelength of interest.

The low-modulus and photo-definable polynorbornene polymer Avatrel 2000P (Promerus, LLC) has been used to fabricate the polymer pillars and sockets. The fabrication of the polymer pillars and sockets involves spin coating of the polymer film, soft baking, exposure of the polymer film through a mask, hard baking, and spray developing. The temperature used for the soft bake and hard bake process steps is 100 °C. Once fabricated, the substrate with the polymer pillars is placed in 200 °C furnace for a thermal cure. Thus, the fabrication of the polymer pillars is a relatively low-temperature process. In Fig. 2(a) and (b), it is shown that the developed fabrication process can be used to fabricate polymer pillars with a very wide range of dimensions and pitches. Polymer pillars with noncircular geometry, including elliptical and rectangular cross sections, have been fabricated. The polymer pillars exhibit very smooth and right-angle sidewalls. The glass transition temperature (T_g) of the polymer is approximately 250 °C making the polymer pillars compatible with the temperatures used for solder bonding. Some of the material requirements for conventional optical interconnects do not necessarily apply to SoPP. For example, we are not restricted to using ultralow

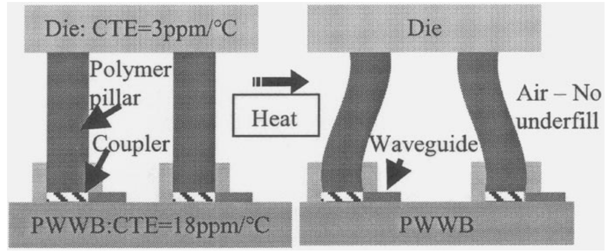

Fig. 4. Schematic illustrating how the polymer pillars compensate the CTE mismatch between the board and the die to minimize optical losses due to offset. Thus, the polymer pillars maintain optical alignment during thermal cycling. The electrical and dual-mode polymer pillars are also mechanically compliant.

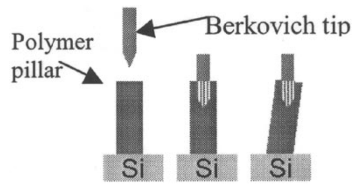

Fig. 5. From left to right: this is a schematic illustrating the measurement setup used to characterize the lateral compliance of a polymer pillar. An 8-mN normal force was used to "stab" the tested polymer pillars.

absorption optical materials due to the short height $(< 200\ \mu\text{m})$ of the polymer pillars.

Because of the low-modulus polymer, the polymer pillars are highly compliant in the lateral direction and, thus, can compensate for the different thermo-mechanical expansions between the die and the PWWB, as schematically illustrated in Fig. 4. Since the I/O interconnections are compliant, the need for underfill during assembly is precluded: The compliant polymer pillars are stress absorbing interconnect structures that undergo strain during thermal cycling. This result is the primary reason why the polymer pillars have an air-cladding. The large Δn caused by the air cladding permits the polymer pillar waveguides to undergo larger bends (for higher displacements) when the CTE mismatches are high. In addition, air does not impose any mechanical–physical constraints on the movement of the highly compliant polymer pillars. The combination of these attributes makes air an ideal cladding for this optical waveguide interconnect technology.

III. Measurements

We have confirmed the high lateral compliance of the polymer pillars experimentally. Using Hysitron's *TriboIndenter* nanomechanical test system, a Berkovich diamond tip was used to "stab" a polymer pillar, as illustrated in Fig. 5. Next, the lateral force-displacement characteristic of the polymer pillar under test was measured up to a peak displacement value of 5 μm. However, the tested polymer pillars were shown to move laterally by approximately 10 μm (peak possible displacement from measurement setup). The measured lateral compliance of a 55-μm-wide and 110-μm-tall circular polymer pillar that is cured at 200 °C for 2 h is approximately 5 μm at 1.7 mN or 3 μm/mN. Increasing the pillar height to approximately 170 μm increases the compliance to more than 5 μm/mN. It was also found that the cure temperature and duration impacted the compliance of the polymer pillars. All lateral deformations

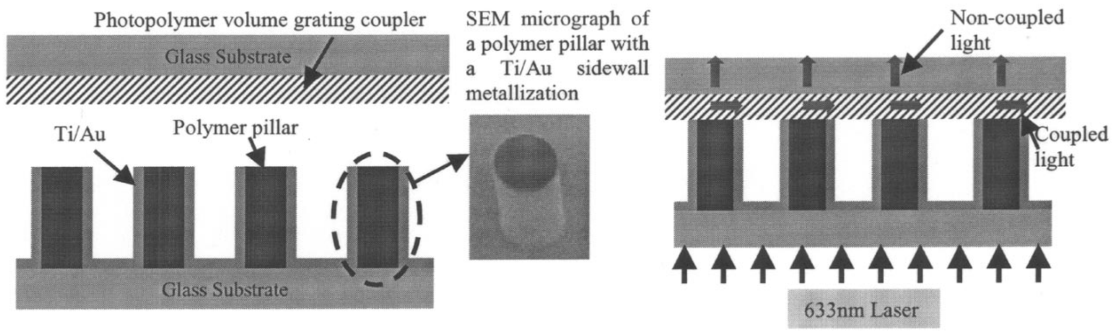

Fig. 6. Schematic of the measurement setup used to demonstrate optical coupling from a set of polymer pillars into a volume grating coupler. The polymer pillars tested were 55 μm wide, 100 μm tall, and on a 325-μm area-array pitch. Coupled light into the photopolymer is $\sim 50\%$.

were elastic and the pillars always moved back to their initial positions following the measurements.

The ability to couple light from a set of polymer pillars into a volume grating coupler has been demonstrated. The measurement configuration is shown in Fig. 6. First, a volume grating coupler of 70% input diffractive efficiency was fabricated on a glass substrate. This nonfocusing grating coupler was fabricated with methods and materials like those reported in [8]. A set of 55-μm-wide and 100-μm-tall polymer pillars were fabricated on a second glass substrate. Next, 300-Å/7000-Å-thick Ti–Au metal films were sputter deposited and patterned such that the metal films covered everything except the tips of the polymer pillars. Thus, the only optically transparent regions on the glass substrate were the 55-μm diameter tips of the pillars, as shown in the SEM micrograph of Fig. 6. Next, the two glass substrates were placed into contact. A 633-nm HeNe laser then illuminated the back side of the glass substrate containing the polymer pillars. The input coupling efficiency as a function of the angular rotation of the two mechanically attached glass substrates was measured to be approximately 50% at near-normal incidence. Not only does this experiment demonstrate the ability to couple light from a set of sidewall metallized polymer pillars into an optical device, such as a diffractive volume grating coupler, but it also demonstrates the principles of wafer-level optical testing and the compatibility of SoPP with such a testing approach.

IV. Conclusion

SoPP is a wafer-level batch fabricated chip I/O interconnection technology. SoPP provides mechanically compliant dual-mode electrical–optical I/O interconnections at high-densities $(>10^5/\mathrm{cm}^2)$ to enable massive chip I/O bandwidth. The lateral compliance minimizes optical losses due to offset and enhances chip reliability. The polymer pillar waveguides make use of optical elements such as mirrors and grating couplers to facilitate the routing of optical signals through right-angle out-of-plane bends. Mechanical measurements demonstrate the high compliance of the polymer pillars. Moreover, the ability to couple light into a volume grating coupler through the polymer pillars was reported.

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